WHAT IS CLAIMED IS:

1. An upconversion and amplification apparatus for use in a transmitter that provides an amplified differential signal having substantially constant output power and containing, over time, data from a plurality of data packets, each data packet including a plurality of training symbols towards a beginning of the packet, the apparatus comprising:

a variable gain amplifier having a variable gain, the variable gain amplifier inputting a differential signal and outputting an amplified differential signal;

a power amplifier electrically coupled to the variable gain amplifier, the power amplifier inputting the differential signal or a signal deriving from the amplified differential signal and outputting a power amplified differential signal having an output power;

a power detection circuit including a power detector that is coupled to the power amplification stage and provides a detected power signal indicating the output power such that the detected power signal is created at an interval that is at least once per symbol during some of the plurality of training symbols; and

a power control circuit electrically coupled to the power detection circuit, and the variable gain amplifier, the power control circuit:

increasing the variable gain of the variable gain amplifier in a step increment if the detected power signal, as detected during each of the some of the plurality of training symbols during each packet transmission, is lower than a predetermined power; and

decreasing the variable gain of the variable gain amplifier in a step decrement if conditions require so that the detected power signal will not exceed an output power threshold.

2. An apparatus according to claim 1, wherein the power control circuit decreases the variable gain after the predetermined power was reached once per packet, at the beginning of the packet prior to the transmission of a first training symbol.

3. An apparatus according to claim 2 wherein the power control circuit maintains the variable gain amplifier at a last gain established at the last of the training symbols used to increase the variable gain for the remainder of a first packet.

4. The apparatus according to claim 1, wherein the power control circuit repeats the increasing the first variable gain in the step increment a maximum of a predetermined number of times for the input differential signal representing each packet of data.

5. The apparatus according to claim 1 whereinthe variable gain amplifier, the power amplifier and the power control circuit are formed on an integrated circuit chip.

6. The apparatus according to claim 1, wherein:

the power detection circuit includes:

two matched power detectors, the power detector that produces a current power detection signal and another power detector that detects a reference power and produces a reference power detection signal; and

a comparator that compares the current power detection signal and the reference power detection signal to determine whether the current output power is below the power threshold or not.

7. The apparatus according to claim 6 wherein the power control circuit strobes the comparator at a predetermined interval to initiate the receiving of the detected power signal.

8. The apparatus according to claim 1 wherein each of the plurality of data packets within the input differential signal contain an initial plurality of known symbol values that are used as a training sequence to more quickly obtain the predetermined power.

9. The apparatus according to claim 1 further including:

a first upmixer that provides a first inductively tuned upconverted differential signal as the input differential signal to the variable gain amplifier; and

a second upmixer electrically coupled between the variable gain amplifier and the power amplifier, the second upmixer inputting the amplified differential signal and outputting a second inductively tuned upconverted differential signal as the signal deriving from the amplified signal;

10. An apparatus according to claim 9, wherein the power control circuit decreases the variable gain after the predetermined power was reached once per packet, at the beginning of the packet prior to the transmission of a first training symbol.

11. An apparatus according to claim 10 wherein the power control circuit maintains the variable gain amplifier at a last gain established at the last of the training symbols used to increase the variable gain for the remainder of a first packet.

12. The apparatus according to claim 9, wherein the power control circuit repeats the increasing the first variable gain in the step increment a maximum of a predetermined number of times for the input differential signal representing each packet of data.

13. The apparatus according to claim 9 wherein the first and second upmixers, the variable gain amplifier, the power amplifier and the power control circuit are formed on an integrated circuit chip.

14. The apparatus according to claim 9, wherein:

the first upmixer upconverts baseband differential signals to intermediate frequency differential signals; and

the second upmixer upconverts the intermediate frequency differential signals to radio frequency differential signals.

15. The apparatus according to claim 9, wherein:

the power detection circuit includes:

two matched power detectors, the power detector that produces a current power detection signal and another power detector that detects a reference power and produces a reference power detection signal; and

a comparator that compares the current power detection signal and the reference power detection signal to determine whether the current output power is below the power threshold or not.

16. The apparatus according to claim 15 wherein the power control circuit strobes the comparator at a predetermined interval to initiate the receiving of the detected power signal.

17. The apparatus according to claim 9 wherein each of the plurality of data packets within the input differential signal contain an initial plurality of known symbol values that are used as a training sequence to more quickly obtain the predetermined power.

18. A method of transmitting digital data packets via a CMOS transceiver with a constant output comprising.

amplifying a first differential analog frequency representation of a first digital data packet containing data values to obtain a first amplified differential analog frequency representation of the first digital data packet, the step of amplifying including amplifying using a variable gain amplifier and amplifying using a power amplifier;

at each of a first plurality of predetermined intervals when amplifying the first differential analog frequency representation of the first digital data packet, determining whether the output power of the first differential analog frequency representation of the first digital data packet reaches a predetermined reference power; and

if the output power does not reach the predetermined reference power during each of the first plurality of predetermined intervals, then incrementing in step increments a gain of the variable gain amplifier at each of the first plurality of predetermined intervals.

19. The method according to claim 18, wherein:

if after the first plurality of predetermined intervals the output power has not reached the predetermined reference power, then amplifying any remaining data values in the variable gain amplifier with a last gain used during the last of the plurality of predetermined intervals.

20. The method according to claim 19, further including the step of:

amplifying a second differential analog frequency representation of a second digital data packet containing second data values to obtain a second amplified differential analog frequency representation of the second digital data packet,

the second differential analog frequency representation of the second digital data packet including a second plurality of predetermined intervals during which the gain in the variable gain amplifier can be changed in the step increments, and wherein at a first interval of the second plurality of predetermined intervals, the gain of the variable gain amplifier is a next step increment from the last gain.

21. The method according to claim 18, wherein:

if, during the first plurality of predetermined intervals the output power has reached an optimal power level based upon a then optimal gain, then, upon receipt of a second differential analog frequency representation of a second digital data packet containing second data values, with the second differential analog frequency representation of the second digital data packet including a second plurality of predetermined intervals during which the gain in the variable gain amplifier can be changed in the step increments, amplifying a first interval

of the second plurality of predetermined intervals with another gain that is reduced from the optimal gain.

22. The method according to claim 21 wherein the another gain is reduced in a user-configurable amount.

23. The method according to claim 21 further including the steps of:

at each of a second plurality of predetermined intervals when amplifying the second differential analog frequency representation of the second digital data packet, determining whether the output power of the second differential analog frequency representation of the second digital data packet reaches the predetermined reference power; and

if the output power does not reach the predetermined reference power during each of the second plurality of predetermined intervals, then incrementing in step increments the gain of the variable gain amplifier at each of the second plurality of predetermined intervals.

24. An apparatus for use in a transmitter comprising:

a variable gain amplifier, the variable gain amplifier including:

an inductively loaded folded cascode circuit that inputs an input differential signal having a VDD-referenced output level and outputs a current;

an input current load circuit that inputs the current from the inductively-loaded folded cascode circuit and outputs an output differential signal having a ground-referenced output level;

a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits; and

a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity to the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode.

25. The apparatus according to claim 24 wherein the positive mode and the negative mode occur at the same time in a gain cell of the variable gain amplifier, thereby providing for fine gain adjustments.

26. The apparatus according to claim 24 wherein the input current load circuit is comprised of four NMOS transistors arranged in a cascode configuration.

27. The apparatus according to claim 26 wherein the input current load circuit is mirrored by each of the plurality of gain cells.

28. The apparatus according to claim 27 wherein each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors.

29. The apparatus according to claim 28 wherein each of the plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode.

30. The apparatus according to claim 24 wherein the input current load circuit is mirrored by each of the plurality of gain cells.

31. The apparatus according to claim 24 wherein each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors.

32. The apparatus according to claim 24 wherein each of the plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode.

33. The apparatus according to claim 24 further comprising:

an intermediate frequency upmixer having a intermediate frequency upmixer output coupled to an input of the variable gain amplifier; and

a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier.